REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 5-9 and 11-13 are active in this case.

In the outstanding Office Action Claims 5, 7-9, 11, and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Feng (U.S. Patent No. 6,417,037) in view of Ahn et al. (U.S. Patent No. 6,383,877, hereinafter Ahn). Claims 6 and 12 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Applicants thank the Examiner for the indication of allowable subject matter in Claims 6 and 12. However, since Applicants believe the present response traverses the prior art rejections of the independent claims, Claims 6 and 12 have been maintained in dependent form. In light of the following comments, it is respectfully requested that the objections to Claims 6 and 12 be withdrawn.

Briefly recapitulating, the semiconductor device as in Claim 5 includes, "first and second transistors located respectively on first and second active regions which are defined by and in direct contact with said isolation insulating film." A first gate insulating film is located on the first active region and a second gate insulating film is located on the second active region. The thickness of the first gate insulating film is greater than the thickness of the second gate insulating film. Further, the isolation insulating film defining and contacting the active regions in Claim 5 has a "recessed portion in an edge portion on the side of said first active region."

Further, Claim 5 defines the depth of the recessed portion around the active region as "a vertical height between a main surface of said first active region and a deepest part of said recessed portion, and is not less than 10 nm." The recessed portion as in Claim 5 is defined with respect to an isolation insulating film to address the problem shown in Figure 13 of the

Applicants' specification. As disclosed by the Applicants, the threshold voltage depends on the depth of the recess around the active region, but there was little understanding of the exact characteristic of the dependency.[1] Therefore, Applicants made a wide range of variations in the depth of the recess to obtain data about the dependency.[2] Applicants then determined that if the recess around the active region is at least 10 nm as recited in Claim 5, there is little variation in the threshold voltage.[3]

The rejection of Claims 5, 7-9, 11, and 13 under 35 U.S.C. § 103(a) as being unpatentable over Feng in view of newly cited reference Ahn is respectfully traversed as discussed below.

As noted in the outstanding Office Action, Feng does not teach a semiconductor device, wherein the isolation film has a recessed portion in an edge portion on the side of the active region.[4] The outstanding Office Action relies on Ahn as teaching "a semiconductor device (Figures 16-21, for example), wherein the isolation film (71) has a first and second recessed portion (T2) in an edge portion on the side of the active region." Further, the outstanding Office Action relies on column 9, lines 3-7 and column 10, lines 6-11 of Ahn as teaching the recessed portion as not being less than 10 nm.[5]

Ahn is directed towards forming a T-shaped isolation region and elevated silicide source/drain regions. More specifically, Ahn forms a T-shaped isolation region in order to prevent a void from being formed when in conventional techniques the entire surface of the semiconductor substrate is planarized after filling of the isolation trench as shown in Figures 1A, 1B, and 2C of Ahn.[6] Further, Ahn discloses a method for forming elevated silicide source/drain regions avoiding the generation of a junction leakage current resulting from the

[1] Applicants' Specification, page 21, lines 10-24.
[2] Id.
[3] Id.
[4] Office Action mailed September 1, 2004, page 2, lines 19-23.
[5] Office Action mailed September 1, 2004, page 3, lines 1-10.
[6] Ahn, column 1, line 35 to column 2, line 7.

silicide layer 26 extending into the boundary between the isolation layer 20 and the source/drain region 25 as shown in II of Figure 5.[7]

Ahn describes a structure in a MOS transistor having an elevated source/drain region, including a T-shaped isolation layer to prevent a silicide layer formed on a source/drain region from causing a junction leakage at the boundary between the isolation layer and the source/drain region. According to the invention described in Ahn, a source/drain region extends to under the head of T-shaped isolation layer by forming an isolation layer as T-shaped. As a result, a thickness of the source/drain region at the boundary between the isolation layer and the source/drain region becomes greater and a junction leakage can be prevented.

Thus, Ahn does not teach or suggest the object or the structure disclosed in the present application, which provides a solution of intentionally deepening the excessively removed portion of the edge portion of the isolation insulating film to form a recess portion to solve the problem of variation in the threshold voltage in a MOS transistor formed by using a dual oxide process, caused by the excessively removed portion of the edge portion of the isolation insulating film defining an active region.

The outstanding Office Action states that Ahn recites forming a trench having a depth from 500 to 4000 Å in the process of forming an T-shaped isolation insulating layer and a depth (thickness) of the head of the T-shaped isolation insulating layer is less than or equal to 1,000 Å.[8] From the above, the outstanding Office Action asserts that Ahn also describes a depth of a recessed portion in an edge portion of an isolation insulating film provided on the side of the first active region is not less than 10 nm, as recited in Claim 5 of the present application.

However, the above-numbers that Ahn discloses merely show a depth of a trench in the process of forming a T-shaped isolation insulating layer and a thickness of a head of a T-shaped isolation insulating layer. Accordingly, Ahn does not teach or suggest forming a recessed

[7] Ahn, column 3, lines 32-53.

portion in an edge portion of a T-shaped isolation insulating layer and the depth of which is not less than 10 nm.

Furthermore, the Examiner states that it would have been obvious to incorporate the teaching of Ahn into the device taught by Feng in order to prevent voids from forming in the isolation layer. However, even if these two references were combined the combination would only provide an isolation insulating layer of Feng as T-shaped, and would not teach or suggest a structure having a recessed portion in an edge portion of a T-shaped isolation insulating layer.

Further, it is not clear why the artisan would be led to modify Feng using the T-shaped isolation regions of Ahn, as the creation of a void in the isolation region of Ahn is taught to occur when the entire semiconductor substrate is planarized after the isolation trench is formed having an aspect ratio greater than or equal to 3, see column 2, lines 41-45. No teaching or suggestion of substrate planarization of isolation trenches having an aspect ratio greater than or equal to 3 is taught by Feng, such that the voids noted at page 3 of the outstanding Office Action would not be a problem. Thus, the rationale offered at page 3, lines 5-10 of the outstanding Office Action of preventing voids, for example, is believed to be without logical support considering the teachings of Ahn and Feng. Further, the problems Ahn addresses with respect to the elevated silicide source/drain regions do not provide motivation for modifying Feng since Feng also does not disclose elevated silicide source/drain regions.

Further, Ahn does not teach or suggest the problem or solution thereto disclosed by the Applicants. Namely, that the threshold voltage depends on the depth of the recess around the active region, and that a recess provided around the active region with a depth of at least 10 nm results in a semiconductor device with little variation in the threshold voltage. To avoid the formation of voids and provide elevated silicide source/drain regions without generating junction leakage current, Ahn discloses that the depth D2 of the upper portion of the T isolation

[8] Office Action mailed September 1, 2004, page 2, line 25 to page 3, line 5.

region should be less than 1,000 Å, which is a range including the 0 to 10 nm in which the Applicants have determined the threshold voltage is highly dependent on the depth of the recess.[9] Therefore, it is apparent that Ahn does not recognize the problem disclosed by the Applicants or the solution thereto, where determining the source of a problem is a consideration pointing to nonobviousness. See, e.g., In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969).

Absent hindsight, there is no motivation to combine Feng in view of Ahn, and the combination would include elevated silicide source/drain regions. Combining only isolated teachings from Ahn with Feng to reconstruct the Applicants' claimed invention is impermissible under 35 U.S.C. § 103. Therefore, the outstanding rejection under 35 U.S.C. § 103(a) is traversed, and it is respectfully submitted that the rejection be withdrawn.

As a result, Feng in view of Ahn does not disclose or suggest the semiconductor device of independent Claim 5 or independent Claim 7. In view of the apparent patentability of Claim 7 for the reasons above noted, it is respectfully submitted that Claims 8, 9, 11, and 13 which depend from Claim 7 are patentably distinguishable over the prior art of record. Applicants respectfully request that the rejection of Claims 5, 7-9, 11, and 13 under 35 U.S.C. § 103(a) as being unpatentable over Feng in view of Ahn be withdrawn. Similarly, it is respectfully requested that the objection to Claims 6 and 12 as being dependent on a rejected base claim be withdrawn.

[9] Ahn, column 10, lines 6-11.

Consequently, in light of the above comments, no further issues are believed to be outstanding in this application, and the present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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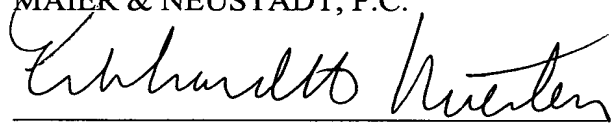

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